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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

S. KONISHI et al

Serial No. 10/658,402

Group Art Unit: 2815

Filed: September 10, 2003

Examiner: Eugene LEE

For: A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

TRANSMITTAL OF CORRECTED FORMAL DRAWINGS

Commissioner for Patents
Mail Stop PGPUB Drawings
P.O. Box 1450
Alexandria, VA 22313-1450

May 13, 2005

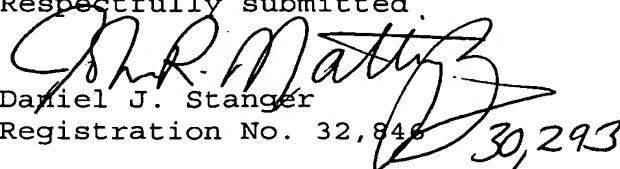
Sir:

Applicants submit herewith two (2) sheets of corrected formal drawings (Figs. 26 and 27). Please substitute the enclosed formal drawings for the originally filed Figs. 26 and 27 drawings. Both sheets of drawings have been marked as "Prior Art" in accordance with the Examiner's objection on Page 2 of the Notice of Allowability mailed February 15, 2005.

None of the other sheets of drawings require correction.

Please charge any additional fees resulting from this action to Deposit Account No. 50-1417.

Respectfully submitted,


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